

# Radiation Characteristics of a 0.11 $\mu$ m Modified Commercial CMOS Process

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**Abstract**—We present radiation data, Total Ionizing Dose and Single Event Effects, on the LSI Logic 0.11  $\mu$ m commercial process and two modified versions of this process. Modified versions include a buried layer to guarantee Single Event Latchup immunity.

**Index Terms**—CMOS digital integrated circuits, Radiation effects, Radiation hardening

## I. INTRODUCTION

THE use of commercial digital foundries could provide a savings in volume, power and weight versus other options for science and spacecraft designs. Application Specific Integrated Circuits (ASIC) offer higher gate densities and increased speed/performance in comparison to circuits built using Field Programmable Gate Arrays (FPGA). Previous evaluation of LSI Logic's 0.18  $\mu$ m CMOS enhanced process showed promising radiation tolerance [1]. We evaluated the radiation performance of LSI Logic's 0.11 $\mu$ m standard CMOS process as well as two modified versions of this process. This paper presents total ionizing dose (TID) and single event effect (SEE) data.

## II. TESTED DEVICES

The tested standard process is a maturing technology that is in volume production today. It is a 0.11  $\mu$ m drawn bulk process with Small Trench Isolation (STI). The core voltage is 1.2V. The technology supports I/O voltages up to 3.3V and up

to 9 metal layers with low K inter metal dielectrics material. The gate oxide thickness is 2.2 nm and the STI thickness is 250 nm. Up to 70 million logic gates can be used on a chip. This process allows ultra high density embedded 6T-SRAM with density over 430 Kbits/mm<sup>2</sup>. LSI Logic's modified versions of this process include a buried layer to guarantee Single Event Latchup (SEL) immunity. Two modified with processes, buried layer 1 and buried layer 2, with two different doping levels of buried layer were tested. Modified processes maintain 100% parametric and functional compatibility with standard process.

Three manufacturer's test vehicles were used. The first two are 4Mbit (512kx8) SRAM memory chip, SRAM-249 and SRAM-187. SRAM-249 uses a high speed SRAM cell. The cell area is 2.49  $\mu$ m<sup>2</sup>. SRAM-187 uses a high density SRAM cell. The cell area is 1.87  $\mu$ m<sup>2</sup>. The minimum cycle time is about 50 ns. The memory core power supply voltage is 1.2V, and the I/O power supply voltage is 2.5V. The SRAM test vehicles are packaged in a 64-lead plastic quad flat pack (PQFP) package.

The third test vehicle is a manufacturer product qualification (PQV) vehicle. PQV includes a logic Qualification chip (Qchip). Qchip contains 384, organized as 6x64, 64-bit Arithmetic and Logic Units (ALU). Each of the ALU 64 bits "a" and "b" input operands, all function control signals and all outputs are registered with a scan type D flip-flop with set and clear. In scan mode, each ALU flip-flop is connected to make a chain of 200 flip-flops. Qchip was tested in scan mode as 6 chains of 200 flip-flops. This design was synthesized to operate at a maximum speed of 20 MHz in scan mode. The memory core power supply voltage is 1.2V, and the I/O power supply voltage is 3.3V. The logic test chip is packaged in a 492 pin plastic enhanced performance ball grid array (EPBGA) package.

## III. EXPERIMENTAL TEST CONDITIONS

TID irradiations were performed with NASA-GSFC Co-60 source. Parts were irradiated up to total dose level of about 300 krad-Si at a dose rate ranging from 0.3 to 18 krad-Si per hour. After irradiation SRAM test vehicles were submitted to a one-week annealing at room temperature. For SRAM test vehicles, 3 parts per process were irradiated with static on

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mode with no pattern loaded before irradiation in the memory devices. For Qchip test vehicle, only one part per process was irradiated in a dynamic on mode with a 1 MHz clock and an alternate input pattern.

In addition to a full functional test, core and I/O standby power supply currents were measured before irradiation and after each irradiation step.

SEE tests were performed at the TEXAS A&M cyclotron with 15 MeV per nucleon heavy ion beams. Test vehicles were tested with NASA-GSFC radiation effect group low cost digital tester (LCDT). LCDT is a reusable universal digital device tester based on Xilinx Spartan 3 Field Programmable Gate Array (FPGA) with input/output (I/O) operation speed up to 200 MHz.

LCDT is the main test board that interfaces with the device under test (DUT)-specific daughter card. The DUT on the daughter card is exercised using the configurable FPGA on LCDT with Hardware Design Language such as VHDL based coding. A remote PC controls LCDT.

- SRAM test vehicle were tested under two different test conditions:
- Static test: a test pattern is loaded in the DUT before irradiation. DUT is irradiated. Then, it is checked after the end of the irradiation run.

Dynamic test: a test pattern is loaded in the DUT before irradiation. During irradiation DUT is continuously read and errors are corrected in real time. Dynamic test was run at a 10MHz clock speed.

For both test modes the detected errors information (address, data read, expected data) were recorded for further analysis. Four different test patterns were tested: all0, all1, checkerboard, and reverse checkerboard.

Qchip test vehicle was tested in scan mode. In this mode, the device is functionally equivalent to 6 shift register chains of 200 flip-flops each. 5 out of the 6 register chains were tested in parallel in the following way: a test pattern is entered in the chain input. The chain output is compared to the test pattern. Errors are counted and error information is stored (clock cycle#, chain number, read bit value, expected bit value). Four different test patterns were used: all0, all1, alternate, and double alternate. Tests were run at different clock speeds from 2 to 16 MHz.

For all test vehicles, the power supply currents of the DUT were monitored and charted during irradiation to detect the occurrence of single event latchup (SEL) or other anomalous condition. In case of SEL, the DUT power supplies are shutdown.

#### IV. TOTAL IONIZING DOSE RESULTS

TID test results on all parts of each process and test vehicle do not show any degradation up to the maximum dose level of 300 krad-Si. No post irradiation effect was observed after one week room temperature annealing. Fig. 1 shows the standby

core supply current of SRAM-187 test vehicle versus total dose.

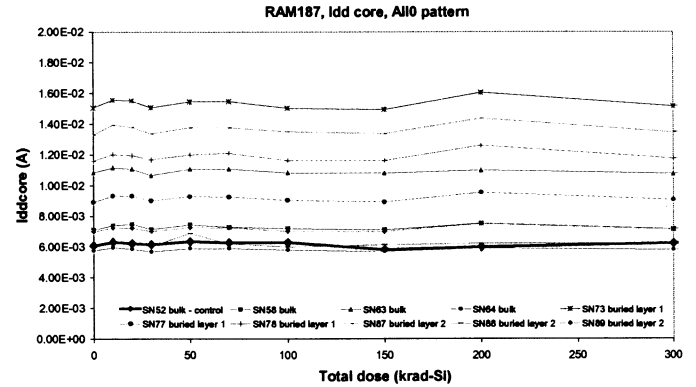


Fig. 1: SRAM-187 test vehicle, core power supply current versus total dose.

#### V. SINGLE EVENT EFFECT TEST RESULTS

##### A. SRAM

Fig. 2 shows the SEL and SEU cross-sections curves for the standard process SRAM test vehicles. Test results show a micro latchup sensitivity at LET higher than 5 MeVcm<sup>2</sup>/mg. Only limited SEU testing was possible because of the micro latchup sensitivity. As the different test modes, test patterns, did not show any significant effect on SEU sensitivity, Fig. 2 shows an average of test results for all different test conditions. We can see in Fig. 2 that at the lowest LET of 2.8 MeVcm<sup>2</sup>/mg the cross-section has not decreased significantly. This indicates a LET threshold well below this value. The maximum measured SEU cross-section at LET of 20 MeVcm<sup>2</sup>/mg is about 2.4 10<sup>-8</sup> cm<sup>2</sup>/bit. There is no significant difference in SEU sensitivity between the two SRAM test vehicles. However, high density test vehicle, SRAM-187, appears to be slightly more sensitive to micro latchup events.

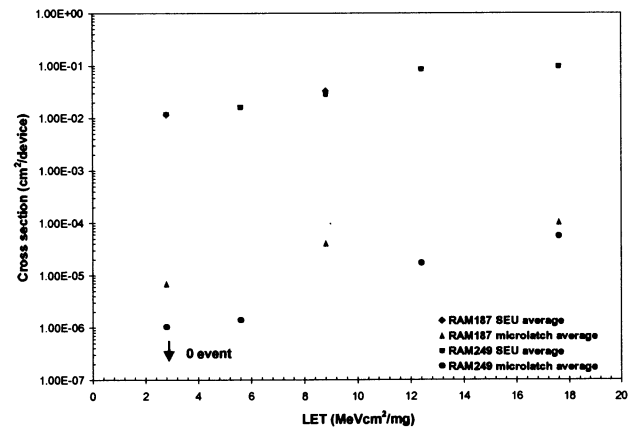


Fig. 2: SRAM, standard process, SEE cross-section curve

When a micro-latchup event occurs, DUT power supply current increases of 6 to 30 mA from the nominal value were noted, and the part shows large cluster of errors until power cycling is performed. Two different types of error clusters

were observed:

- One column of a bit slice is in error. Fig. 3 shows an example of a column error. This error indicates a micro latchup in the sense/amp area.
- One to successive 64 bits in a column are in error. Only one column or up to the 16 columns of a bit slice may show the same errors. Fig. 4 shows an example of this error pattern. This error indicates a micro latchup in the memory array because of an insufficient number of substrate ties.

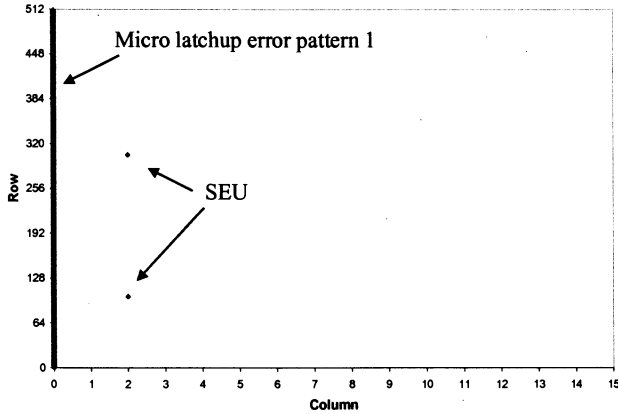


Fig. 3: example of a column error in a bit slice, (1 bit slice=8Kbit organized as 512 rows by 16 columns).

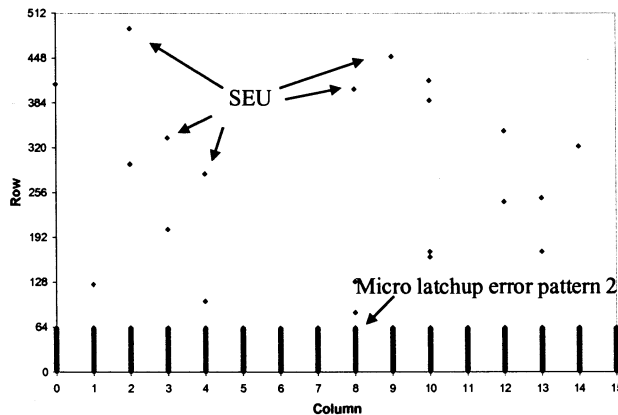


Fig.4: Example of an error pattern, 64 successive bits in the 16 columns of a bit slice are in error.

The two processes with buried layer did not show any micro latchup or latchup events sensitivity up to the maximum tested LET of 108 MeVcm<sup>2</sup>/mg and a test fluence of 10<sup>7</sup> ions/cm<sup>2</sup>. Fig. 5 shows the SRAM-249 SEU cross-section curves for the three different processes. We can see that bulk process is the more sensitive process and buried layer 2 process is the less sensitive process. Maximum measured SEU cross-section is about 8 10<sup>-8</sup> cm<sup>2</sup>/bit. High-density devices, SRAM-187, are slightly more sensitive than the high-speed devices, SRAM-249. We can see in Fig. 5 that cross-section curves do not show any saturation. This indicates diffusion effects where a single particle affects multiple neighboring cells.

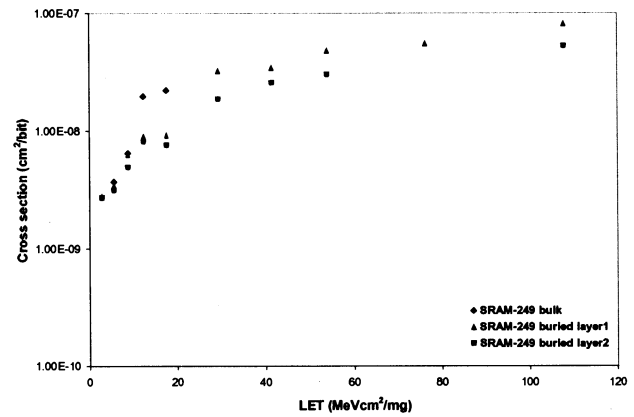


Fig. 5: SRAM-249, SEU cross-section curves

At low LET the number of multiple event upsets (MEU) is very low. Fig. 6 shows the location of errors at the lowest LET of 2.8 MeVcm<sup>2</sup>/mg in one of the 16 8Kx32 bits blocks of SRAM-187 buried layer 1. During this irradiation run 61 SEU and only one MEU were observed in this 8Kx32 bits SRAM block. The MEU affected two neighboring cells.

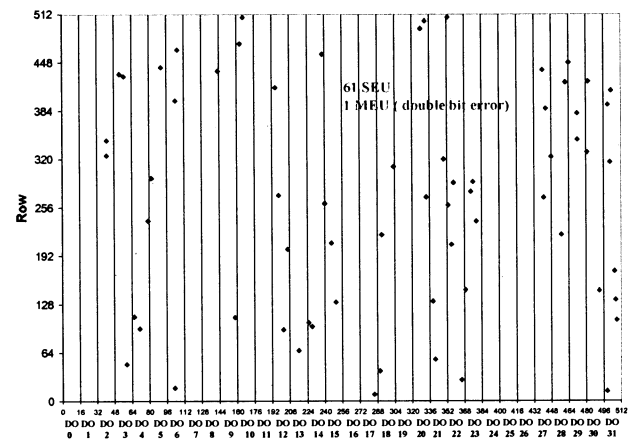


Fig. 6: SRAM-187 buried layer 1, mapping of errors within one memory block at LET of 2.8 MeVcm<sup>2</sup>/mg. 4M SRAM are made of 16 blocks of 8Kx32 bits (32 bit slices)

At high LET there are more MEU than SEU. Fig. 7 shows the location of errors at the highest LET of 108 MeVcm<sup>2</sup>/mg in one of the 16 blocks of SRAM-187 buried layer 1. Even though about the same number of memory cells are in errors in the examples shown in Fig. 6 and Fig. 7 the distribution of errors is different. In addition to single bit errors distributed randomly in the memory array, we see in Fig. 7 a large number of error clusters distributed randomly in the memory array. During this irradiation run 14 SEU and 17 MEU were observed. Most MEU affect two neighboring cells. The largest MEU observed had 4 neighboring cells in error.

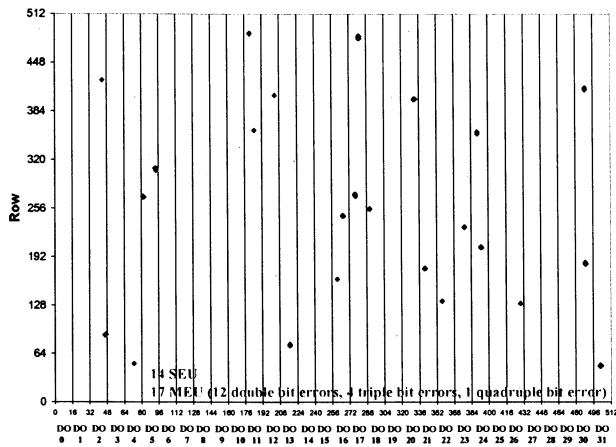


Fig. 7: SRAM-187 buried layer 1, mapping of errors within one memory block at Let of 108 MeVcm<sup>2</sup>/mg

### B. Qchip

No SEL or micro latchup were observed on Qchip test vehicle for the three processes up to the maximum tested LET of 108 MeVcm<sup>2</sup>/mg. SEU and Single Event Transients (SET) were observed. SET that propagated to flip-flop clock, set, or reset inputs caused burst errors. Flip-flops set and reset signals are asynchronous. Therefore, all SET reaching these inputs can be observed whatever the test frequency. With alternate and double alternate patterns, all SET reaching flip-flops set, reset, or clock inputs were observed. With all0 pattern only SET reaching flip-flops set input were observed. With all1 pattern only SET reaching flip-flops reset input were observed. We observed burst errors because of SET in clock, set and reset inputs. Bursts affected all the 200 flip-flops in a chain in most cases. Fig. 8 shows the cross-section curves for the total numbers of errors (bursts + SEU) and SEU only. As the different test modes and test patterns did not show any significant effect on SEU sensitivity, Fig. 8 shows an average of test results for all different test conditions. No significant difference can be seen between the three processes. SET sensitivity is significant. Maximum measured cross-section for the total number of errors at LET of 108 MeVcm<sup>2</sup>/mg is  $6 \cdot 10^{-7}$  cm<sup>2</sup>/flip-flop. It is 10 times larger than SEU cross-section. At the lowest LET of 2.8 MeVcm<sup>2</sup>/mg, near the LET threshold, cross-section for the total number of errors is 5 times larger than SEU cross-section.

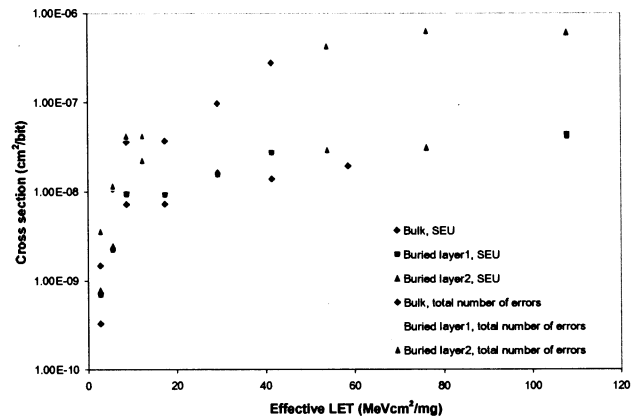


Fig. 8: Qchip, SEE cross-section curves

## VI. CONCLUSION

As expected, for a 0.11  $\mu$ m CMOS process, the TID tolerance is good. No noticeable degradation was observed up to a total dose of 300 krad-Si. SEE test results show that the commercial bulk process is sensitive to micro latchup event for the high-density designs. This is the most striking result of this study. Even with a 1.2V core supply voltage, commercial technologies can still be sensitive to latchup or micro-latchup events. Modified processes with a buried layer are not sensitive to micro latchup events. SET sensitivity is high. SET increase the overall Qchip sensitivity by a factor 10.

## ACKNOWLEDGMENT

## REFERENCES

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